APPARATUS AND METHOD FOR PERFORMING ADDITION OF PKG RECODED NUMBERS

BACKGROUND OF THE INVENTION

TECHNICAL FIELD

The present invention generally relates to an apparatus for performing arithmetic operations, and more particularly, to reducing noise production and power consumption by performing the addition of PKG recoded numbers.

DESCRIPTION OF RELATED ART

Generally, traditional dual-rail encoding (i.e. mousetrap logic) is often implemented in arithmetic circuitry. Dual-rail encoding requires that multiple wires be enabled to indicate the proper value. For power and noise reasons, it is desirable to reduce the number of wires routed over an integrated circuit and the switching activity of these wires. Therefore, PKG recoding can be implemented to reduce the number of wires and the switching activity of these wires.

Illustrated in FIG. 1 is a recoding table 2 illustrating the encoding of two logical values into mousetrap logic. The mousetrap logic values are then encoded into PKG recoding values to reduce the number of wires routed over an integrated circuit from 4 wires to 3 wires. There is also a large savings in the switching activity of these wires. The switching activity is reduced from 2 of 4 wires switched to 1 of 3 wires switched, as shown

by recoding table 2. These reductions cause the significant savings of cutting power consumption by 50% and the area for wiring by 25%.

Illustrated in FIG. 2A is a block diagram representing the dual rail pairs of signals for values A 3(A&B) and B 4(A&B) being recoded into PKG

5   signals (101-103) by recoding device 9.

Illustrated in FIG. 2B is a block diagram of a possible example of a mousetrap logic encoding circuit 11 for P-propagate code in a PKG recoding. As shown in FIG. 2B, the propagate code 101 is generated from the mousetrap encoding by taking the logical "AND" operation of the high

10   A 3B mousetrap encoded signal and the low B 4A mousetrap encoded signal in the "AND" logic 12. The output from the "AND" logic 12 is one input into the "OR" logic 14. The logical "AND" of the low A 3A mousetrap encoded sign and the high B 4B mousetrap encoded signal is performed in the "ADD" logic 13, and is input as the second input into "OR" gate 14.

15   The final logical operation utilizing the "OR" 14 produces the P-propagate code 101 that is equal to the logical end of the A high 3B and B low 4A, or the A low 3A and B high 4B signals.

Illustrated in FIG. 2C is a block diagram of a possible example of a mousetrap logic encoding circuit 16 for K-kill code 102 in PKG recoding.

20   The kill or clear all bits code in the PKG recoding is represented by a logical "AND" of the A low 3A and B low 4A mousetrap encoding bits. If both the A low 3A and B low 4A bits are enabled, the PKG recoding generates a K code 102, indicating the clearing of both logical bits A 4 and B 5.

Illustrated in FIG. 2D is a block diagram of a possible example of a mousetrap logic encoding circuit 18 for the G-generate code 103 in PKG recoding. The G-generate code 103 in PKG recoding, is constructed utilizing a logical end of the A high 3B and B high 4B bits in mousetrap encoding. If the A high 3B and B high 4B bits are enabled, the PKG recoding will generate a G code 103 that indicates the setting of both bits.

While using PKG recoded signals can reduce the number of wires needed to represent two values, it does cause the problem of how to add numbers in this PKG recoded form. Thus, a heretofore-unaddressed need exists in the industry to address the aforementioned deficiencies and inadequacies.

SUMMARY OF THE INVENTION

The present invention provides an apparatus and method for performing the addition of PKG recoded numbers.

Briefly described, in architecture, the system can be implemented as follows. An apparatus is configured to receive a first value and a second PKG value, and generating a sum value and a carry value from the first value and second PKG value.

The present invention can also be viewed as providing a method for reducing noise production and power consumption by performing the addition of PKG recoded numbers. In this regard, the method can be broadly summarized by the following steps: (1) receiving a first value and

second PKG value, and (2) generating a sum value and a carry value from the first value and second PKG value.

Other features and advantages of the present invention will become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional features and advantages be included herein within the scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. 1 is a table illustrating a PKG encoding method that reduces switching activity of lines by 50% over traditional domino encoding.

FIG. 2A is a block diagram illustrating the encoding circuit for PKG recoding.

FIG. 2B is a block diagram illustrating a mousetrap logic encoding circuit for P-propagate code in a PKG recoding.

FIG. 2C is a block diagram illustrating a mousetrap logic encoding circuit for K-kill code in a PKG recoding.

FIG. 2D is a block diagram illustrating a mousetrap logic encoding circuit for the G-generate code in a PKG recoding.

FIG. 3A is block diagram of an example of a carry save adder of the present invention, for performing addition on a newly encoded PKG input and a traditional binary bit.

FIG. 3B is a block diagram of an example of a circuit to generate the sum output of the redesigned carry save adder of the present invention as shown in Fig. 3A.

FIG. 3C is a block diagram of an example of a circuit for generating the carry output of the redesigned carry save adder of the present invention as shown in Fig. 3A.

FIG. 4 is a block diagram of an example of a redesigned carry save adder of the present invention, for adding two PKG recoded numbers.

FIG. 5 is a table illustrating an example of PKG encoding signals for two PKG recoded numbers.

FIG. 6 is a block diagram of an example of an adder of the present invention, for adding two PKG recoded numbers.

FIG. 7 is a schematic of a possible example of a two PKG recoded number adder circuit, generating the carry out low signals of the present invention.

FIG. 8 is a schematic of a possible example of a two PKG recoded number adder circuit, for generating the carry out high signal of the present invention.

FIG. 9 is a schematic of a possible example of a two PKG recoded number adder circuit, for generating the G signal output of the present invention.

FIG. 10 is a schematic of a possible example of a two PKG recoded

5   number adder circuit of the present invention, for generating a P signal output.

FIG. 11 is a schematic of a possible example of a two PKG recoded number adder circuit of the present invention for generating the K signal output.

10   FIG. 12 is a schematic of a possible example of a PKG recoded carry save adder of the present invention for generating the sum high and sum low signals.

FIG. 13 is a schematic of a possible example of a PKG recoded carry save adder of the present invention for generating the carry high and carry

15   low signals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the description of the invention as illustrated in the drawings. While the invention will be

20   described in connection with these drawings, there is no intent to limit it to the embodiment or embodiments disclosed therein. On the contrary, the intent is to cover all alternatives, modifications, and equivalents included within the spirit and scope of the invention as defined by the appended claims.

Illustrated in Fig. 3A is a block diagram of a possible example of a

carry save adder 100 redesigned for performing addition on a newly

encoded PKG input and a traditional binary bit. As can be seen in FIG.

3A, the P 101, K 102 and G 103 signals are received by the modified carry

5 save adder 100. The P 101, K 102 and G 103 signals are input along with

carry-in signal CI 104, representing one traditional binary bit carry-in

number.

The signals are processed by the modified carry save adder 100 and

output is generated as sum 106 and carry 107 signals. The sum 106

10 signal is representative of an exclusive "OR" between the P 101 propagate

signal and the carry-in signal CI 104. The logic circuit to generate the sum

signal 106 is herein defined in further detail with regard to FIG. 3B.

The carry signal is generated from a logical "AND"ing of the P 101

and carry-in CI 104 signals. This added combination of carry-in CI 104

15 and P 101, is then "OR"ed with the G 103 signal to generate the carry

signal 107. The logic circuit to generate the carry signal 107 is herein

defined in further detail with regard to FIG. 3C.

Illustrated in FIG. 3B is a block diagram of a possible example of a

sum output generation circuit 111 to generate the sum signal 106, of the

20 redesigned carry save adder 100 of the present invention, as shown in Fig.

3A. Shown in FIG. 3B, the carry-in signal CI 104 is exclusively "OR"ed

with the P signal 101 using the logical exclusive "OR" circuit 112 to

generate the sum signal 106, as shown in Fig. 3A.

Illustrated in FIG. 3C is a block diagram of a possible example of a carry output generation circuit 113 for generating the carry signal 107 of the redesigned carry save adder 100 of the present invention, as shown in Fig. 3A. As shown, the carry-in signal CI 104 and the P signal 101 are

5 added together in logical "AND" gate 114. The output of the logical "AND" gate 114 is input into the logical "OR" gate 115. Also input into the logical "OR" gate 115, is the G signal 103. The output of a logical "OR" gate 115 is the carry signal 107, as shown in Fig. 3A.

Illustrated in FIG. 4 is a block diagram of a modified carry save

10 adder 120 for adding two PKG recoded numbers. The two number PKG carry save adder 120, adds two numbers in PKG form and produces a PKG number with a traditional binary bit carry-out signal. The first PKG recoded number 121-123 is input into the carry save adder 120. The second PKG number 124-126 is also input into the carry save adder 120.

15 The carry save adder generates an output PKG signal 101-103 from the pair of PKG recoded numbers. Also generated is a traditional binary bit carry-out signal C2 127.

Illustrated in FIG. 5, is a table 140 explaining by one example, signals generated by the addition of two PKG encoding signals. As shown,

20 table 140 defines the various input (121-126) and output values (127 & 131-133). The output values (127 & 131-133) are generated by the PKG adding circuit of the present invention, by adding two PKG recoded numbers (121-123) and (124-126). The PKG adding circuit for adding two

PKG recoded numbers is herein defined in greater detail with regard to Fig. 6.

The formulas described below are utilized by the PKG adding circuit of the present invention, to generate the desired output values from the

5   two PKG recoded numbers P1, K1 & G1 (121-123) and P2, K2 & G2 (124-126), are as follows.

$$P = P1 \bullet (K2 + G2) + P2 \bullet (K1 + G1)$$

$$K = (K1 \bullet K2) + (K1 \bullet G2) + (K2 \bullet G1)$$

$$G = (P1 \bullet P2) + (G1 \bullet G2)$$

10    $$C2 = G1 + G2$$

$$\overline{C2} = (K1 + P1) \bullet (K2 + P2)$$

Illustrated in FIG. 6 is a block diagram of the PKG adding circuit

15   150 of the present invention, for adding two PKG recoded numbers. The PKG adding circuit 150 adds two numbers in PKG form by utilizing the carry save adder 100 and carry save adder 120 in series. The carry save adder 100 and carry save adder 120, were previously defined with regard to FIGS. 3A and 4.

20   As can be seen, the addition of two numbers in PKG form is broken into two parts, the first part being the input of the two PKG recoded numbers P1, K1 & G1 (121-123) and P2, K2 & G2 (124-126). The carry save adder 120 generates the PKG signals 131-133 and carry output 127. The PKG signals 131-133 are input into carry save adder 100 along with

25   the carry-input signal 134 from a previous addition. The carry save adder

100 adds the signals and generates a dual rail encoded sum output 146 and carry output 147 signals.

Illustrated in FIG. 7 is a circuit schematic of a portion of a possible example of the PKG adding circuit 150, of the present invention. Shown,

5 is the portion of the two PKG recoded number carry save adder 120, that generates the dual-rail carry-out low (C2L) 127A signal. The dual-rail carry-out low (C2L) 127A signal, is utilized in the example PKG adding circuit 150 of the present invention, for adding two PKG recoded numbers.

Illustrated in FIG. 8 is a circuit schematic of a portion of a possible

10 example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the two PKG recoded number carry save adder 120, that generates the dual-rail carry-out high (C2H) 127B signal. The dual-rail carry-out high signal (C2H) 127B signal is utilized in the example PKG adding circuit 150, of the present invention, for adding two PKG recoded

15 numbers.

Illustrated in FIG. 9 is a circuit schematic of a portion of a possible example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the two PKG recoded number carry save adder 120, that generates the PKG G 133 signal. The PKG G 133 signal is utilized in the

20 example PKG adding circuit 150, of the present invention, for adding two PKG recoded numbers.

Illustrated in FIG. 10 is a circuit schematic of a portion of a possible example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the two PKG recoded number carry save adder 120, that

generates the PKG P 131 output signal. The PKG P 131 signal is utilized in the example PKG adding circuit 150, of the present invention, for adding two PKG recoded numbers.

Illustrated in FIG. 11 is a circuit schematic of a portion of a possible
5 example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the two PKG recoded number carry save adder 120, with the example PKG adding circuit 150 that generates the PKG K 132 signal. The PKG K 132 signal is utilized in example PKG adding circuit 150, of the present invention, for adding two PKG recoded numbers.

10 Illustrated in FIG. 12 is a circuit schematic of a portion of a possible example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the possible example of a PKG carry save adder 100 circuit (FIG. 3A). This schematic of a possible example of a PKG carry save adder 100 circuit (FIG. 3A), is used for generating the dual-rail sum low (SOL)
15 146A and high (SOH) 146B signals in the possible example of the PKG adding circuit 150 (FIG. 4), of the present invention. The inputs P 131, K 132, G 133 and CIL 134 (A &B) are obtained from the output of an example two PKG recoded numbers PKG carry save adder 120, illustrated by functional circuit (FIG. 4) and schematics (FIGS 7-11).

20 Illustrated in FIG. 13 is a circuit schematic of a portion of a possible example of the PKG adding circuit 150, of the present invention. Shown, is the portion of the possible example of a PKG carry save adder 100 circuit (FIG. 3A). This schematic of a possible example of a PKG carry save adder 100 circuit (FIG. 3A), is used for generating the dual-rail carry-out low

(COL) 147A and high (COH) 147B signals in the possible example of the PKG adding circuit 150 (FIG. 4), of the present invention. The inputs P 131, K 132, G 133 and CIL 134 (A &B) are obtained from the output of two PKG recoded numbers PKG carry save adder 120, illustrated by functional circuit (FIG. 4) and schematics (FIGS 7-11).

Certainly a designer of ordinary skill in the art could produce a gating cell similar to those shown in FIGs. 7-13 to implement the example PKG adding circuit 150 of the present invention.

The block diagrams of Figs. 2(A-D)-4 and 6-13 show the architecture, functionality, and operation of a possible implementation of the system architecture to increase the performance of PKG carry save adder operations. In this regard, each block represents a module, device, or logic. It should also be noted that in some alternative implementations, the functions noted in the blocks might occur out of the order. For example, two blocks may in fact be executed substantially concurrently, depending upon the functionality involved.

It should be emphasized that the above-described embodiments of the present invention, particularly, any "preferred" embodiments, are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the invention without departing substantially from the spirit and principles of the invention. All such modifications and variations are intended to be

included herein within the scope of the present invention and protected by the following claims.